Amendments to the Specification

Please replace the paragraph beginning on page 17, line 4, with the following rewritten paragraph:

In Fig. 8, an internal circuit 50 of an IC has at least an ID generation circuit 51 which generates an ID, an ID write circuit 52 for writing the ID in response to a reset signal input through an terminal 56 and a command end signal input through a terminal 57, and a built-in memory 53 used as a cache memory or the like. The ID of the IC chip is generated by the ID generation circuit ~~101~~ 51 and stored in a designated address of the built-in memory 53 by the ID write circuit 52. The address is designated on the basis of address data stored in an address register 54 for writing the ID which is provided in the internal circuit 50 of the IC. The address register 54 for writing the ID is connected to an external CPU 210 through a connection terminal 58. The external CPU 210 changes the address data. The built-in memory 53 is connected to the external CPU 210 through a connection terminal 59. The ID is read by the external CPU 210, and firmware 211 which is one type of software that recognizes the ID. The firmware 211 appropriately controls the IC by specifying the production history, ~~manufacture's~~ manufacturer's number, and the like of the IC chip.

B1

Please replace the paragraph beginning on page 17, line 23, with the following rewritten paragraph:

Details of the ID write operation will be described. In the present embodiment, the ID is also written when the reset signal is released after the power-on reset. However, the following description focuses on the write operation at the end of the command. The CPU 210 sets the ID write address to the address register 54 for writing the ID before the IC performs command operations. As the ID write address, an area in which general data is not stored is selected. When the command operation of the IC ends, the command end signal is active for a predetermined period of time. In response to this, the ID write circuit 52 sets the

B2

address signal of the built-in memory 53 to the ID write address, and sets the read/write signal of the built-in memory 53 to "write". The ID write circuit ~~12~~ 52 then turns on a chip select signal of the built-in memory 53, whereby the ID is written into the designated address of the built-in memory 53.

B2